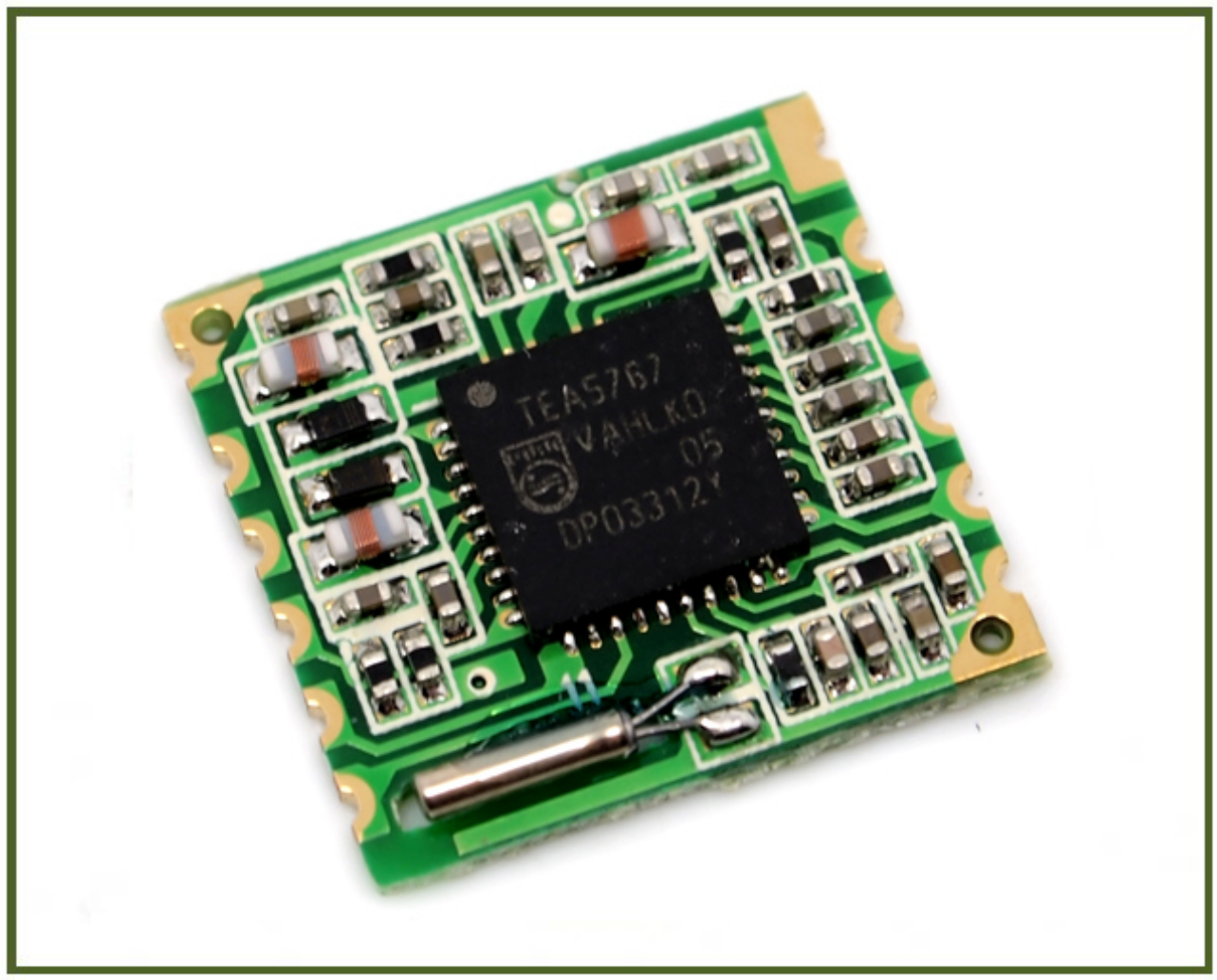
# PLL FM Stereo Radio(Receiver) Module

## 88MHz ~ 108MHz

Related Product : (PLL FM Stereo radio Transmitter Module)



## 1. PLL FM Stereo Radio(Receiver) Module.

* This is a PLL FM Stereo Audio Receiver Module that picks up wireless signals/FM broadcast signals over 76-108MHz, having same functions as domestic FM Radio set(Radio & Receiver).
* While generally used receivers work on a single or several pre-determined frequencies, it can pick up any stereo signals of any frequency within the range of 76-108MHz.
* Miniature-sized to fit into any of your products, it is especially easy to install in electronic devices of compact size.
* It can serve as a miniature-size receiver itself.

## 2. Features.

. Stereo reception from all broadcast band(76-108MHz)
. PLL system guarantees good frequency stability.
. Miniature-sized(SMD Type), easy to apply to your products.
. Controllable from CPU(MCU).
. Works on a single voltage 5V.

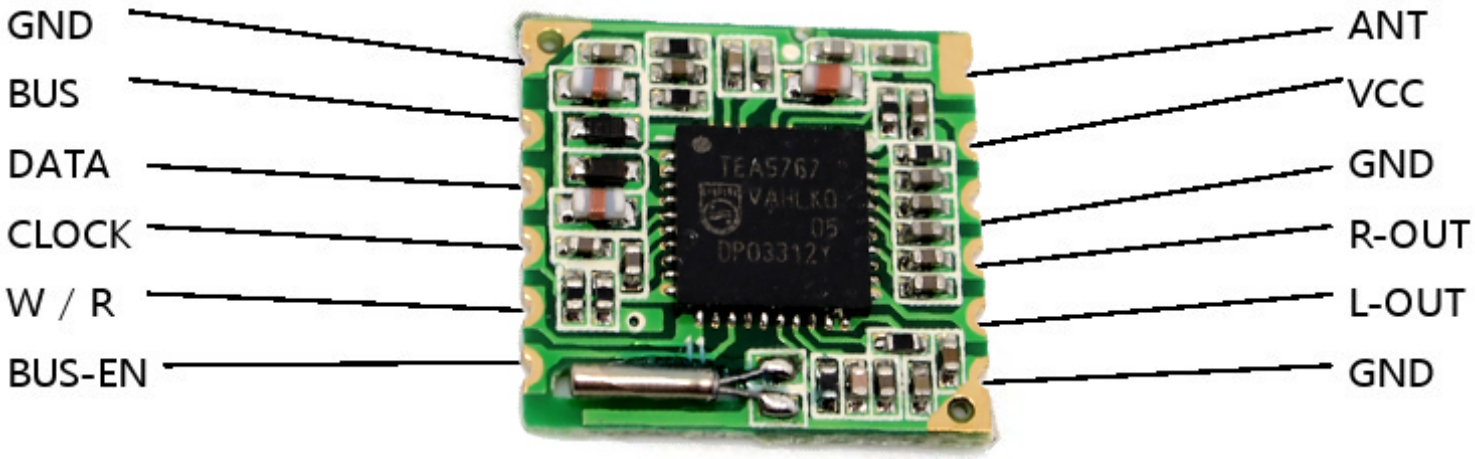
## 3. Applications

. Small Size FM Radio.
. Portable TV.
. MP3, PDA.
. Telephone & Mobile.
. CAR Navigation.
. Game machine.

## 4. PLL FM Stereo Radio(Receiver) Module Specification.

| Item | Specification |
|---|---|
| Operation Voltage | DC 3V, (Max DC 5V) |
| Operation Current | 8 - 15mA |
| Frequency | 88MHz ~ 108MHz |
| Receiving Method | Super Heterodyne |
| Audio Output Power | 60 – 90mV |
| Control | CPU (MCU) : 3-Wire Bus |

## 5. PLL FM Stereo Radio(Receiver) Module Pin Information.

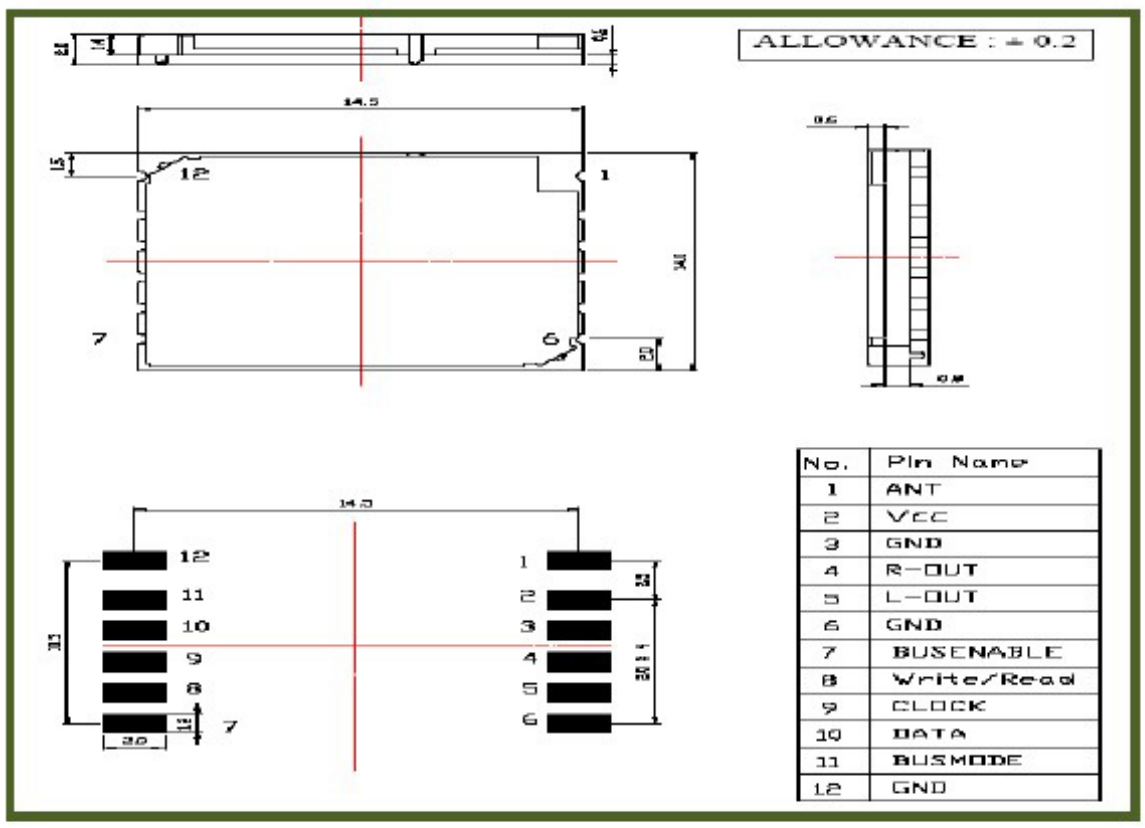



* ANT : Antenna Connect.
* VCC : DC 3V~5V (+) Input.
* R-OUT : Audio Right Signal Output.
* L-OUT : Audio Left Signal Output.
* GND : Power (-) Connect.
* BUS, DATA, CLOCK, W/R, BUS-EN : CPU (MCU) Control.

. Please use the NR-B108 Only Antenna (PN-ANT-FM) or FM Frequency Antenna.

. The sound from R-OUT/L-OUT is output small, so to get bigger sound connect audio amplifier to output.(as amplifiers, you can use general audio amps like LM386 etc.)

## 6. PLL FM Stereo Radio(Receiver) Module Size.




| No. | Pin Name |
|---|---|
| 1 | ANT |
| 2 | Vcc |
| 3 | GND |
| 4 | R-OUT |
| 5 | L-OUT |
| 6 | GND |
| 7 | BUSENABLE |
| 8 | Write/Read |
| 9 | CLOCK |
| 10 | DATA |
| 11 | BUSMODE |
| 12 | GND |

## 7. PLL FM Stereo Radio(Receiver) Module Specification.

General Specifications.

| NO | Item | SPEC |
|---|---|---|
| 1 | Frequency Range | 76 ~ 108 ㎒ |
| 2 | Receiving System | Upper Super Heterodyne System |
| 3 | Intermediate frequency | 225 ㎑ |
| 4 | Operating Temperature | -20 ~ +70 ℃ |
| 5 | ANT Input Impedance | 40 Ω Unbalanced |

Test Modulation

| NO | Item | M O N O | S T E R E O |
|---|---|---|---|
| 1 | Modulation Frquency | 1㎑, 22.5㎑/dev | 1㎑, 75㎑/dev<br>PILOT=10% fpil=19㎑ |
| 2 | RF Input level | 60dBμV | |
| 3 | TEST frequency | 90㎒ | |

DC Specification

| I T E M | Test condition | SPEC | | | |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | UNIT |
| Supply Voltage(Vcc) | Off station | 2.5 | 3.0 | 5.0 | V |
| Consumption Current | - | 8.0 | 11.5 | 15.0 | mA |

Electrical Specification

| NO | I T E M | Test condition | SPEC | | | |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | UNIT |
| 1 | Usable Sensitivity<br>(S/N 30 dB) | 76.0 ㎒ | - | 8 | 15 | dBμV |
| | | 90.0 ㎒ | - | 8 | 15 | dBμV |
| | | 106.0 ㎒ | - | 8 | 15 | dBμV |
| 2 | S/N Ratio | with B.P.F<br>300Hz to 15KHz | 54 | 60 | - | dB |
| 3 | Distortion | with B.P.F<br>300Hz to 15KHz | - | 0.5 | 1.5 | % |
| 4 | Distortion<br>with Strong Signal | with B.P.F<br>120 dBμV | - | 1 | 3.0 | % |
| 5 | Audio Ouput Level | 1㎑, 22.5㎑/dev | 60 | 75 | 90 | mVr |
| 6 | 3dB Limiting | 90.0 ㎒ | - | 12 | 20 | |
| 7 | Image Rejection | 90.0 ㎒ | 24 | 28 | - | dB |
| 8 | Stereo Separation | | 22 | 25 | - | dB |

Standard test condition.

Temperature : 20 ± 2 ℃

Relative humidyty : 65 ± 5 %

Tolerance of supply voltage : ± 0.05 V

Tolerance of tuning voltage : ± 0.005 V or less

However, test may be done within the following condition.

Temperature : 20 ± 15 ℃

Relative humidyty : 65 ± 20 %

Tolerance of supply voltage : ± 0.1 V

Tolerance of tuning voltage : ± 0.01 V

Calibration

| Receiving frequecy | Tuning voltage | Allowable voltage |
|---|---|---|
| [㎒] | [V] | [V] |
| 76.0 | | Vcc-0.2 Max |
| 87.5 | | - |
| 98.0 | | - |
| 108.0 | | 0.20 Min |

## 8. PLL FM Stereo Radio(Receiver) Module Control Format.

Table 1 Write mode

| DATA BYTE 1 | DATA BYTE 2 | DATA BYTE 3 | DATA BYTE 4 | DATA BYTE 5 |
|---|---|---|---|---|

Table 2 Format of 1st data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| MUTE | SM | PLL13 | PLL12 | PLL11 | PLL10 | PLL9 | PLL8 |

Table 3 Description of 1st data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 | MUTE | if MUTE = 1 then L and R audio are muted; if MUTE = 0 then L and R audio are not muted |
| 6 | SM | **Search Mode:** if SM = 1 then in search mode; if SM = 0 then not in search mode |
| 5 to 0 | PLL[13:8] | setting of synthesizer programmable counter for search or preset |

Table 4 Format of 2nd data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| PLL7 | PLL6 | PLL5 | PLL4 | PLL3 | PLL2 | PLL1 | PLL0 |

Table 5 Description of 2nd data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 to 0 | PLL[7:0] | setting of synthesizer programmable counter for search or preset |

Table 6 Format of 3rd data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| SUD | SSL1 | SSL0 | HLSI | MS | ML | MR | SWP1 |

Table 7 Description of 3rd data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 | SUD | **Search Up/Down:** if SUD = 1 then search up; if SUD = 0 then search down |
| 6 and 5 | SSL[1:0] | **Search Stop Level:** see Table 8 |
| 4 | HLSI | **HIGH/LOW Side Injection:** if HLSI = 1 then HIGH side LO injection; if HLSI = 0 then LOW side LO injection |
| 3 | MS | **Mono to Stereo:** if MS = 1 then forced mono; if MS = 0 then stereo ON |
| 2 | ML | **Mute Left:** if ML = 1 then the left audio channel is muted and forced mono; if ML = 0 then the left audio channel is not muted |
| 1 | MR | **Mute Right:** if MR = 1 then the right audio channel is muted and forced mono; if MR = 0 then the right audio channel is not muted |
| 0 | SWP1 | **Software programmable port 1:** if SWP1 = 1 then port 1 is HIGH; if SWP1 = 0 then port 1 is LOW |

Table 8 Search stop level setting

| SSL1 | SSL0 | SEARCH STOP LEVEL |
|---|---|---|
| 0 | 0 | not allowed in search mode |
| 0 | 1 | low; level ADC output = 5 |
| 1 | 0 | mid; level ADC output = 7 |
| 1 | 1 | high; level ADC output = 10 |

Table 9 Format of 4th data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| SWP2 | STBY | BL | XTAL | SMUTE | HCC | SNC | SI |

Table 10 Description of 4th data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 | SWP2 | **Software programmable port 2:** if SWP2 = 1 then port 2 is HIGH; if SWP2 = 0 then port 2 is LOW |
| 6 | STBY | **Standby:** if STBY = 1 then in standby mode; if STBY = 0 then not in standby mode |
| 5 | BL | **Band Limits:** if BL = 1 then Japanese FM band; if BL = 0 then US/Europe FM band |
| 4 | XTAL | if XTAL = 1 then $f_{xtal}$ = 32.768 kHz; if XTAL = 0 then $f_{xtal}$ = 13 MHz |
| 3 | SMUTE | **Soft MUTE:** if SMUTE = 1 then soft mute is ON; if SMUTE = 0 then soft mute is OFF |
| 2 | HCC | **High Cut Control:** if HCC = 1 then high cut control is ON; if HCC = 0 then high cut control is OFF |
| 1 | SNC | **Stereo Noise Cancelling:** if SNC = 1 then stereo noise cancelling is ON; if SNC = 0 then stereo noise cancelling is OFF |
| 0 | SI | **Search Indicator:** if SI = 1 then pin SWPORT1 is output for the ready flag; if SI = 0 then pin SWPORT1 is software programmable port 1 |

Table 11 Format of 5th data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| PLLREF | DTC | – | – | – | – | – | – |

Table 12 Description of 5th data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 | PLLREF | if PLLREF = 1 then the 6.5 MHz reference frequency for the PLL is enabled; if PLLREF = 0 then the 6.5 MHz reference frequency for the PLL is disabled |
| 6 | DTC | if DTC = 1 then the de-emphasis time constant is 75 µs; if DTC = 0 then the de-emphasis time constant is 50 µs |
| 5 to 0 | – | not used; position is don't care |

## 8.3 Reading data

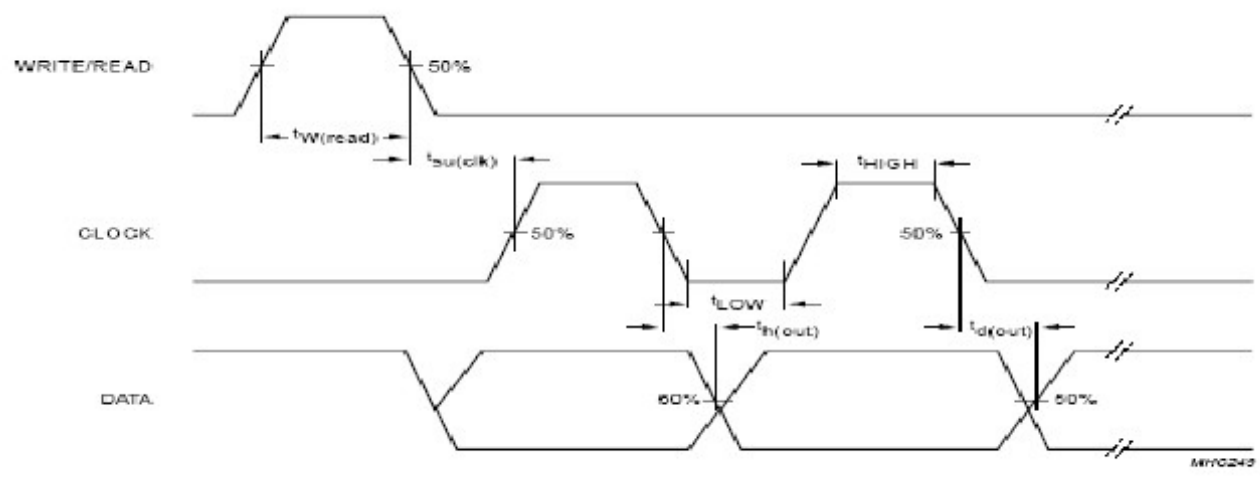



Fig.4 3-wire bus read data.

Table 13 Read mode

| DATA BYTE 1 | DATA BYTE 2 | DATA BYTE 3 | DATA BYTE 4 | DATA BYTE 5 |
|---|---|---|---|---|

Table 14 Format of 1st data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| RF | BLF | PLL13 | PLL12 | PLL11 | PLL10 | PLL9 | PLL8 |

Table 15 Description of 1st data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 | RF | **Ready Flag:** if RF = 1 then a station has been found or the band limit has been reached; if RF = 0 then no station has been found |
| 6 | BLF | **Band Limit Flag:** if BLF = 1 then the band limit has been reached; if BLF = 0 then the band limit has not been reached |
| 5 to 0 | PLL[13:8] | setting of synthesizer programmable counter after search or preset |

Table 16 Format of 2nd data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| PLL7 | PLL6 | PLL5 | PLL4 | PLL3 | PLL2 | PLL1 | PLL0 |

Table 17 Description of 2nd data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 to 0 | PLL[7:0] | setting of synthesizer programmable counter after search or preset |

Table 18 Format of 3rd data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| STEREO | IF6 | IF5 | IF4 | IF3 | IF2 | IF1 | IF0 |

Table 19 Description of 3rd data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 | STEREO | Stereo indication: if STEREO = 1 then stereo reception; if STEREO = 0 then mono reception |
| 6 to 0 | PLL[13:8] | IF counter result |

Table 20 Format of 4th data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| LEV3 | LEV2 | LEV1 | LEV0 | CI3 | CI2 | CI1 | 0 |

Table 21 Description of 4th data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 to 4 | LEV[3:0] | level ADC output |
| 3 to 1 | CI[3:1] | Chip Identification: these bits have to be set to logic 0 |
| 0 | – | this bit is internally set to logic 0 |

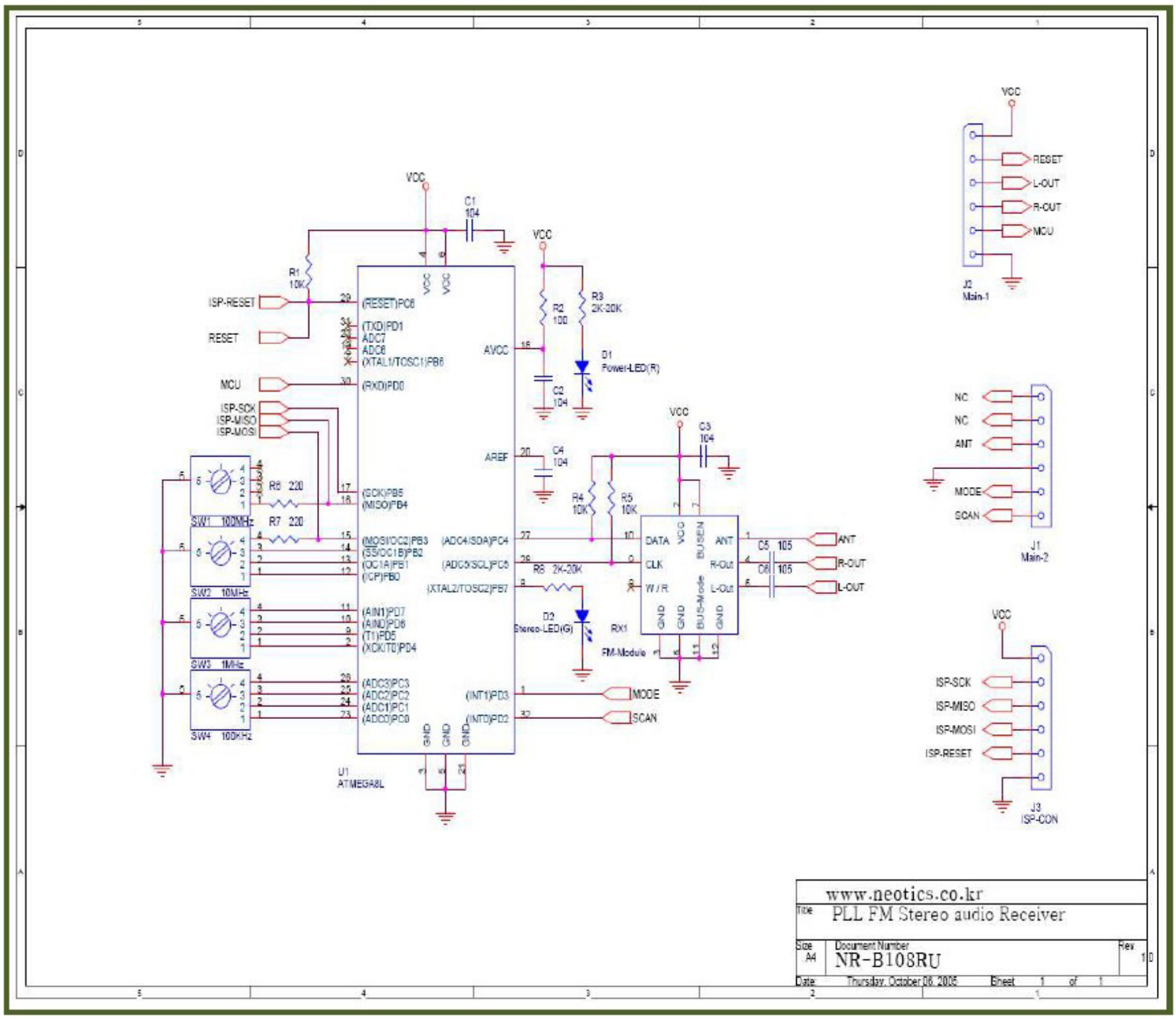
Table 22 Format of 5th data byte

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 23 Description of 5th data byte bits

| BIT | SYMBOL | DESCRIPTION |
|---|---|---|
| 7 to 0 | – | reserved for future extensions; these bits are internally set to logic 0 |

## 9. PLL FM Stereo Radio(Receiver) Module Test Circuit.




### ***** Caution *****

1. Check the features first to connect with other equipment.
2. This circuit is strictly tested.
3. The developer, manufacturer or dealer is not responsible for any malfunctioning/damage caused by connection with other equipment.
4. Appropriate permit /approval is required for some products utilizing this module, depending on functions and usages.